REMARKS

The Office Action dated August 15, 2006 has been received and considered. In this response, claims 1, 5, and 24 have been amended to correct antecedent basis and correct typographical errors. These amendments do not narrow the scope of the claims and therefore do not require additional consideration. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Withdrawal of Restriction Requirement

The Applicants note with appreciation the withdrawal of the previous Restriction Requirement and the examination of all pending claims.

Objection to Claims 22 and 24

At page 2 of the Office Action, claim 22 is objected to for lacking antecedent basis and claim 24 is objected to for a typographical error. Claim 22 has been amended to correct its dependency, which also provides sufficient antecedent basis, and claim 24 has been amended consistent with the Examiner's suggestion. Reconsideration and withdrawal of this objection therefore is respectfully requested.

Anticipation Rejection of Claims 1, 11-13 and 24

At page 3 of the Office Action, claims 1, 11-13 and 24 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jones et al. (U.S. Patent No. 6,415,344). This rejection is respectfully traversed.

Independent claim 1 recites the features of "executing at a processor core module of a system on a chip (SOC) a first MSR access command, the first MSR access command comprising a first destination address and a first destination data." Independent claim 24 recites the similar features of "a means for executing at a first MSR access command, the first MSR access command comprising a first destination address and a first destination data." The Office Action asserts that these features are disclosed by Figure 6 of Jones and the passage of Jones at col. 8, lines 22-24. *Office Action*, p. 3. The Applicants respectfully disagree. Figure 6 of Jones illustrates "a format of a digital signal request packet" (see Jones, col. 2, lines 52-53) and the cited passage of Jones merely provides that the data signal request packet format of FIG. 6

includes a destination indicator 73. Jones, col. 8, lines 22-24. However, Jones fails to disclose, or even suggest, that the data signal request packet represented by Figure 6 of Jones is a MSR (machine specific register) access command. Further, Jones fails to disclose executing a MSR access command in any manner. Accordingly, as Jones fails to disclose executing an MSR access command, Jones necessarily fails to disclose the claimed features of "executing at a processor core of a SOC a first MSR access command" as recited by claim 1 and the similar features recited by claim 24.

Independent claim 1 also recites the features of "providing, in response to executing the first MSR access command, a first access request to an external bus port to access an external device, the first access request including the first destination address and the first destination data and the external device being external the SOC." Independent claim 24 recites similar features. The Office Action asserts that Figure 1 of Jones and the passage of Jones at col. 4, lines 39-53 disclose these features. For ease of reference, the cited passage of Jones is reproduced below:

> The CPU's can be operated in conventional manner receiving instructions from the instruction caches 42 on chip and effecting data read or write operations with the data cache 43 on chip. Additionally external memory accesses for read or write operations may be made through the external memory interface 32 and bus connection 33. The debug port 30 is described in more detail in FIGS. 2 to 5. As shown in FIG. 2, this circuitry includes a hard reset controller 45 connected to a hard reset pin 46. The controller 45 is connected to all modules on the chip shown in FIG. 1 so that when the hard reset signal is asserted on pin 46 all circuitry on the chip is reset.
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> As will be described below, this port 30 provides an important external communication which may be used for example in debugging procedures. The on-chip CPU's 12 and 13 may obtain instruction code (by memory access packets) for execution from an external source communicating through the port 30. Furthermore, event packets providing either interrupts or control signals may be put onto the P-link 15 from an external chip via the port 30. Communications on the P-link system 15 are carried out in bit parallel format. Transmissions on the data bus 20 of the P-link 15 may be carried out in multiple byte packets, for example 35 bytes for each packet, so that one packet is transmitted in five consecutive eight byte transfers along the P-link each transfer being in bit parallel format. The port 30 is arranged to reduce the parallelism of packets obtained from the P-link 15 so that they are output in bit serial format through the output 31 or alternatively in a much reduced parallel format relative to that used on the P-link 15 so as to reduce the number of external connection pins needed to implement the external connection 31.

Jones, col. 4, lines 39-67.

Contrary to the assertions of the Office Action, this passage of Jones, as well as the remainder of the disclosure of Jones, fails to disclose or suggest providing a first access request to an external bus port to access an external device in response to executing a first MSR access command as recited by claim 1 and similarly recited by claim 24, nor does this cited passage disclose or suggest that the first access request includes the first destination address and the first destination data of the MSR access command as provided by claims 1 and 24.

Claims 11-13 depend from claim 1. Jones therefore fails to disclose the combinations of features of claims 11-13 at least by virtue of this dependency. Moreover, these claims recite additional features not disclosed by Jones. To illustrate, claim 12 recites the additional features of "accessing a first external peripheral when the first destination address has a first value; and accessing a second external peripheral when the first destination address has a second value." Contrary to the assertions of the Office Action, the passage of Jones at col. 8, lines 24-29 cited by the Office Action with respect to claim 12 fails to disclose or suggest that different external peripherals are accessed depending on whether the first destination address has a first value or a second value.

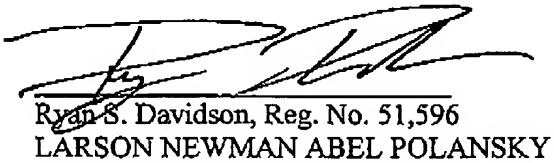
In view of the forgoing, it is respectfully submitted that the anticipation rejection of claims 1, 11-13, and 24 s improper. Reconsideration and withdrawal of this rejection therefore is respectfully requested.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicants believe no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 01-0365.

Respectfully submitted,



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